

10/528255

Rec'd PCT/PTO 17 MAR 2005

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

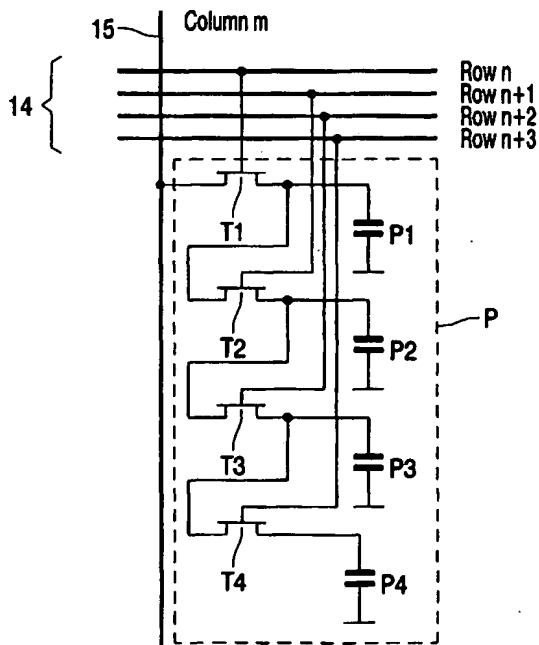
(19) World Intellectual Property
Organization
International Bureau(43) International Publication Date
1 April 2004 (01.04.2004)

PCT

(10) International Publication Number
WO 2004/027748 A1

- (51) International Patent Classification⁷: G09G 3/36 (74) Agent: WILLIAMSON, Paul, L.; Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).
- (21) International Application Number: PCT/IB2003/003974 (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (22) International Filing Date: 12 September 2003 (12.09.2003) (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
0222039.0 23 September 2002 (23.09.2002) GB
0305634.8 12 March 2003 (12.03.2003) GB
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- Published:
— with international search report
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: ACTIVE MATRIX DISPLAY DEVICES



(57) Abstract: In an active matrix display device, such as an AMOLED, having an array of pixels (P) addressed via sets of row and column conductors (14, 15) to which, respectively, selection and data signals are applied, each pixel comprises a plurality of sub pixels (P1 - P4) which each have an associated switch, for example a TFT, (T1 - T4) and which are addressed with data signals through a common switch (T1) coupled to a column conductor (15). Addressing the sub pixels through a common switch reduces the effective capacitance of the column conductor. By appropriate control of the switches (T1 - T4) the pixels can be driven in a first mode in which the common switch (T1) is operated to control the simultaneous addressing of the sub pixels (P1 - P4) with a data signal, for example, for a video display with full grey scale capability, and in a second mode in which the switches (T1 - T4) are controlled sequentially to allow different data signals to be applied to the individual sub pixels, for example, as required for a low power standby mode of operation with limited grey scale and colour capability.

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